REMARKS/ARGUMENTS

Claim 1-23 are pending in the present application. The applicant hereby traverses the examiner's rejection of the respective claims. Therefore, all of the present claims are in their original form, and are presented for convenience of review.

Request for information under 37 U.S.C. 1.105

The applicant submits that information further describing prior solutions described in paragraph [0004] of the present application is unknown or cannot be readily obtained at the time of filing the present response.

Drawings objected to under 37 CFR 1.83(a)

The examiner states that enable signals for logical AND gates 315 and logical AND gates 350, as described in par. [0028] of the specification and referenced in FIG. 3, are not shown. The examiner also states that the logical AND gates 315 and the logical AND gates 350 have multiple inputs from the multiplexers 312 and the spreaders 340, respectively. The applicant believes that the examiner's confusion for both of these concerns lies in the fact that the enable signals (e.g., test_ovsf_gen_en(0) for logical AND gate 315, and test_pn_sel(0) for the logical AND gate 350), as shown in FIG. 3, are sourced by the microprocessor and not by the multiplexers 312 and the spreaders 340, as described in par. [0028] of the specification and more accurately referenced in informal drawing of FIG. 3, which was originally submitted. In other words, the left side of the lines, representing the enable signals, should not be touching the multiplexers 312 and the spreaders 340. This appears to be a "typographical" error in the formal drawing of FIG. 3, which was not present in the original informal drawing of FIG. 3. A new replacement sheet is provided to better show a space between the left side of the lines, representing the enable signals, and the multiplexers 312 and the spreaders 340.

The examiner states that the components in block 210 in FIG. 2 do not have labels and that the multiplexers in block 210 do not have control inputs. The applicant has amended FIG. 2 to provide labels and control inputs. The applicant has also amended the specification to include a description for the new labels. Note that the control of each multiplexer in block 210 is present represented by the logical "0" and "1" labeled on each multiplexer. Therefore, such control was already explicitly described in FIG. 210.

Rejection under 35 USC 112, second paragraph

The examiner rejected claims 7-10, 18-19, and 23 under 35 USC 112, second paragraph, as being indefinite for failing to point out and distinctly claim the subject matter which the applicant regards as the invention.

The applicants submits that claims 7, 18, and 23 are definite for the following reasons. Claim 7, for example, is dependent on claim 1, and not one of claims 3-7, as perhaps considered by the examiner. Therefore, the claimed limitation: "a plurality of scrambling codes and a plurality of spreading codes to form the plurality of codes" introduces new elements "a plurality of scrambling codes and a plurality of spreading codes" to form "the plurality of codes" as originally introduced in claim 1. Claim 3 introduces the limitation: "plurality of codes comprises a scrambling code and a spreading code" which are further described in claims 4-6, but claims 3-6 are not linked to claim 7. Similar reasons apply to claims 18 and 23.

Rejection under 35 USC 102

Claims 1-4, 13-16, and 20-22 are rejected under 35 USC 102(a) as being anticipated by Rahul Chauhan (a web site reference cited on Form 892).

The Applicant respectfully traverses the rejection for the following reasons.

35 USC 102(a) states: "A person shall be entitled to a patent unless —

(a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for patent."

The web site, cited by the examiner, notes a copyright of 2002 by Rahul Chauhan and a last update on 8:24 PM 7/1/2003. Under the link for "A Walk Through to IS-95A, CDMA-2000 And Call Processing," the quoted document describes "Version 2 June 20, 2003." Therefore, it is not clear from the web site reference or the linked document when the particular information cited by the examiner was first described by Rahul Chauhan.

The present application was filed on December 30, 2003, and the oath or declaration for the present application was signed on December 30, 2003. Therefore, the particular information cited by the examiner in the publication of Rahul Chauhan in the year 2000, June

20, 2003, or July 1, 2003 may not be "before the invention thereof by the applicant for patent," as required by 35 USC 102(a). If necessary, the Applicant reserves the right to overcome the present rejection under 35 U.S.C. 102(a) by showing that Rahul Chauhan's dates are after the date of invention by the applicant for patent.

In "A Walk Through to IS-95A, CDMA-2000 And Call Processing," Rahul Chauhan teaches conventional call processing for CDMA, including a description of a "forward link" on pages 9-11 as follows.

"The user data is spread to a channel chip rate of 1.2288 MHz. IS-95 uses a different modulation and spreading technique for the forward and reverse links. On the forward link, the base station simultaneously transmits the user data for all mobiles in the cell by using different spreading sequence for each mobile. The user data is encoded, interleaved, and spread by one of sixty-four orgthogonal spreading sequences (Walsh functions). To avoid interference, all signals in a particular cell are scrambled using a pseudorandom sequence of length 215 chips." (under point 11, at the bottom of page 9)

In summary of Rahul Chauhan, the base station applies the spreading sequence (Walsh functions) and the scrambled code (pseudorandom sequence) to a transmit signal, which is transmitted to a mobile station.

Rahul Chauhan's description of conventional CDMA does not teach or suggest "a test data pattern generator configured to spread an input test data with at least one of the plurality of codes to form a spread test data, and to provide the spread test data to the demodulator," as claimed in claim 1, for example, for the following reasons.

Rahul Chauhan does not teach or suggest a "test data pattern generator."

The claimed "test data pattern generator" is not the same as Rahul Chauhan's "base station."

The claimed "spread an input test data" is not the same as Rahul Chauhan's "user data is spread." In other words "input test data" is not the same as "user data."

The claimed "spread test data" is not the same as Rahul Chauhan's "spread user data."

Further, claim 1 claims, at least: "A code division multiple access (CDMA) integrated circuit, comprising: a demodulator … and a test data pattern generator."

Therefore, both the demodulator and the test data pattern generator are in the same integrated circuit. Although each of a conventional CDMA base station and a conventional CDMA mobile station typically includes a demodulator, the signal that is demodulated was transmitted from a CDMA mobile station (i.e., reverse link) and a CDMA base station (i.e., forward link), respectively.

By contrast, claim 1 claims, at least, "provide the spread test data to the demodulator." By the nature of the claim construction in claim 1, the claimed "the spread test data to the demodulator" is provided to the demodulator in the same "CDMA integrated circuit" that comprises the "test data pattern generator."

In other words, in Rahul Chauhan, the base station transmits spread user data to a remotely-located mobile station over the forward link. By contrast, in claim 1, the claimed "test data pattern generator" provides "the spread test data to the demodulator" in the same "CDMA integrated circuit."

Arguments analogous to those for claim 1 also apply to independent claims 13 and 20. Further, the respective dependent claims should be allowable because of their dependency on presumably allowable independent claims.

The present invention advantageously generates realistic test data patterns without an external test data pattern generator, and without significant increase to the CDMA chip hardware and complexity.

Rejection under 35 USC 103

Claims 5, 6, 12, and 17 are rejected under 35 USC 103(a) as being unpatentable over Rahul Chauhan (a web site reference) as applied to claims 3, 11, and 15, and further in view of Bertin, et al. (US Patent 6802033) ("Bertin").

As succinctly stated in the MPEP, to establish a prima facie case of obviousness, three basic criteria must be satisfied:

"First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine the teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must

teach or suggest all the claimed limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art and not based on the applicant's disclosure." Section 706.02(j) (citing *In re Vaeck,* 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991)).

"To support the conclusion that the claimed invention is directed to obvious subject matter, either the references must expressly or impliedly suggest the claimed invention or the examiner must present a convincing line of reasoning as to why the artisan would have found the claimed invention to have been obvious in light of the teachings of the references." MPEP 706.02(j) (quoting *Ex parte Clapp*, 227 USPQ 972, 973 (Bd. Pat. App. & Inter. 1985)).

For the reasons stated under the rejection under 35 USC 102(a), as applied to independent claims 1, 13, and 20, the applicant submits that the combination of Rahul Chauhan and Bertin render dependent claims 5, 6, 12, and 17 unpatentable.

In view of the foregoing, Applicant submits that all pending claims are in condition for allowance. Applicant respectfully requests the reconsideration and reexamination of this application and the timely allowance of the pending claims. Should any issues remain unresolved, the Examiner is encouraged to telephone the undersigned at the number provided below.

If there are any other fees due in connection with the filing of the response, please charge the fees to our Deposit Account No. 17-0026. If a fee is required for an extension of time under 37 CFR 1.136 not accounted for above, such an extension is requested and the fee should also be charged to our Deposit Account.

Applicants therefore respectfully request that a timely Notice of Allowance be issued in this case.

Respectfully submitted,

Dated: November 28, 2006

By: /Donald C. Kordich/
Donald C. Kordich
Attorney for Applicant
Registration No. 38,213

QUALCOMM Incorporated
5775 Morehouse Drive
San Diego, California 92121-2779
Telephone: (858) 658-5928
Facsimile: (858) 658-2502